WHAT IS CLAIMED IS:

1. A method for connecting an integrated circuit to a substrate, the method comprising

providing a first electrical contact structure on the integrated circuit,

providing a second electrical contact structure on the substrate,

at least one of the first and second electrical contact structures having an elastic elevation thereon,

attaching the integrated circuit to a frame structure,

forming a current path between the first electrical contact structure and the second electrical contact structure, and

attaching the frame structure to the substrate, thereby compressing the elastic elevation.

2. The method according to claim 1, further comprising providing a lateral subregion in said frame structure,

the lateral subregion at least partially surrounding the integrated circuit.

3. The method according to claim 2, further comprising selecting

said subregion to include a peripheral annular region.

4. The method according to claim 2, further comprising selecting

said subregion to include an interrupted support region.

5. The method according to claim 2, wherein

said subregion is not in contact with a surface of said substrate when said current path is formed.

6. The method according to claim 5, further comprising

applying heat to bring said frame structure in contact with said substrate, such that upon heating said subregion expands and touches a surface of said substrate, and upon cooling said subregion remains attached to the surface of said substrate.

7. The method according to claim 1, further comprising

providing a compression stop region on one of said integrated circuit and said substrate.

8. The method according to claim 1, further comprising
providing metallization on the elastic elevation.

9. The method according to claim 2, further comprising providing,
on said frame structure, a planar base region that protrudes laterally beyond the integrated circuit, and connecting
said subregion to the base region such that a space exists between said subregion and said integrated circuit.

10. The method according to claim 1, further comprising
forming a unitary frame structure in which the subregion and a base region are integral with each other.

11. The method according to claim 2, further comprising
adhesively bonding said subregion to said substrate.

12. The method according to claim 2, further comprising
soldering said subregion to said substrate.

13. The method according to claim 1, further comprising
bringing said first electrical contact structure and said second electrical contact structure into mechanical contact, such that
said first electrical contact structure and said second electrical contact structure are displaceable with respect to each other in a common plane.

14. The method according to claim 1, further comprising
disposing said elastic elevation on said first electrical contact structure.

15. The method according to claim 14, wherein providing
the second electrical contact structure has a planar terminal region.

16. The method according to claim 15, further comprising
selecting a material having a thermal expansion coefficient of the planar terminal region to be greater than the thermal expansion coefficient of the elastic elevation.

17. A circuit arrangement comprising

a first electrical contact structure on the integrated circuit,

a corresponding second electrical contact structure on the substrate,

the first electrical contact structure being in electrical communication with the second electrical contact structure,

at least one of the first and second electrical contact structures having an elastic elevation thereon,

a frame structure attached to the integrated circuit and the substrate and being disposed to compress the elastic elevation.

thereby compressing the elastic elevation.

18. A circuit arrangement according to claim 17, wherein

said frame structure includes a lateral subregion at least partially surrounding the integrated circuit.

19. A circuit arrangement according to claim 17, wherein
said subregion includes a peripheral annular region.

20. A circuit arrangement according to claim 17, wherein
said subregion includes an interrupted support region.

21. A circuit arrangement according claim 17, further comprising
a compression stop region on said integrated circuit.

22. A circuit arrangement according to claim 17, further comprising
a metallization layer on the elastic elevation.

23. A circuit arrangement according to claim 17, further comprising a planar base region on said frame structure, wherein

said subregion is connected to a base region protruding laterally beyond the integrated circuit such that a space exists between said integrated circuit and the subregion.

24. A circuit arrangement according claim 17, wherein
said frame structure is a unitary piece.

25. A circuit arrangement according to claim 17, further comprising,
an adhesive between said substrate and said frame.

26. A circuit arrangement according to claim 17 further comprising,
a solder between said substrate and said frame.

27. A circuit arrangement according claim 17, wherein
said first electrical contact structure and said second electrical contact structure are in mechanical contact, and
said first electrical contact structure and said second electrical contact structure are displaceable with respect to each other in a common plane.

28. A circuit arrangement according claim 17, wherein
said elastic elevation is connected to said first electrical contact structure.

29. A circuit arrangement according claim 28, wherein
said second electrical contact structure has a planar terminal region.

30. A circuit arrangement according to claim 29, wherein
the planar terminal region has a thermal expansion coefficient greater than a thermal expansion coefficient of the elastic elevation.